The documentation and process conversion measures necessary to comply with this document shall be completed by 18 April 2007.

INCH-POUND

MIL-PRF-19500/323K
18 January 2007
SUPERSEDING
MIL-PRF-19500/323J
6 December 2004

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, PNP, SILICON, SWITCHING,
TYPES 2N3250A, 2N3251A, 2N3250AUB, 2N3251AUB,
JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for PNP silicon switching transistors. Four levels of product assurance are provided for each device type as specified in MIL-PRF-19500. Two levels of product assurance are provided for die.

1.2 Physical dimensions. See figure 1 (similar to TO-18), 2 (UB), and 3 (die) herein.

1.3 Maximum ratings, unless otherwise specified, T_C = + 25°C.

Type	P_T (1) T_{PCB} = +25°C	P_T (1) T_C = +25°C	P_T (1) T_{SP} = +25°C	$R_{\theta J(PCB)}$ (2)	$R_{\theta JC}$ (2)	$R_{\theta JSP}$ (2)	V_{CBO}	V_{CEO}	V_{EBO}	I_C	T_J and T_{STG}
	mW	mW	mW	°C/W	°C/W	°C/W	V dc	V dc	V dc	mA dc	°C
2N3250A	360	360	N/A	325	150	N/A	60	60	5.0	200	-65 to +200
2N3251A	360	360	N/A	325	150	N/A	60	60	5.0	200	
2N3250AUB	360	N/A	360	325	N/A	95	60	60	5.0	200	
2N3251AUB	360	N/A	360	325	N/A	95	60	60	5.0	200	

(1) For derating, see figures 4, 5, and 6.
(2) For thermal impedance curves, see figures 7, 8, and 9.

Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil .

1.4 Primary electrical characteristics.

Limits	h_{FE1} V_{CE} = 1.0 V dc I_C = 0.1 mA dc		h_{FE3} (1) V_{CE} = 1.0 V dc I_C = 10 mA dc		h_{FE4} (1) V_{CE} = 1.0 V dc I_C = 50 mA dc		$\|h_{fe}\|$ f = 100 MHz V_{CE} = 20 V dc; I_C = 10 mA dc	
	Min	Max	Min	Max	Min	Max	Min	Max
2N3250A, AUB	40		50	150	15		2.5	9.0
2N3251A, AUB	80		100	300	30		3.0	9.0

Limits	$r_b'C_C$ V_{CE} = 20 V dc I_C = 10 mA dc f = 31.8 MHz	$V_{CE(SAT)1}$ I_C = 10 mA dc I_B = 1.0 mA dc	C_{obo} V_{CB} = 10 V dc I_E = 0 100 kHz ≤ f ≤ 1 MHz	t_{on} I_C = 10 mA dc I_B = 1.0 mA dc	t_{off} I_C = 10 mA dc I_B = 1.0 mA dc		N_F V_{CE} = 5 V dc I_C = .1 mA dc Rg = 1kΩ f = 100 Hz
					2N3250A, 2N3250AUB	2N3251A, 2N3251AUB	
	ps	V dc	pF	ns	ns	ns	dB
Min	5						
Max	250	0.25	6	70	250	300	6

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

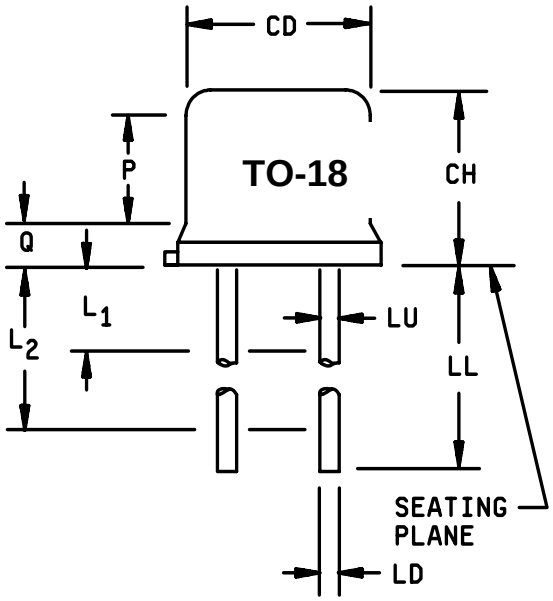
DEPARTMENT OF DEFENSE STANDARDS

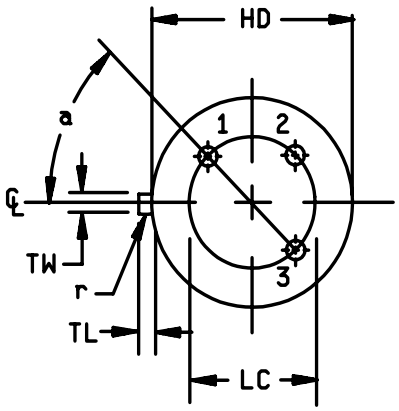
MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

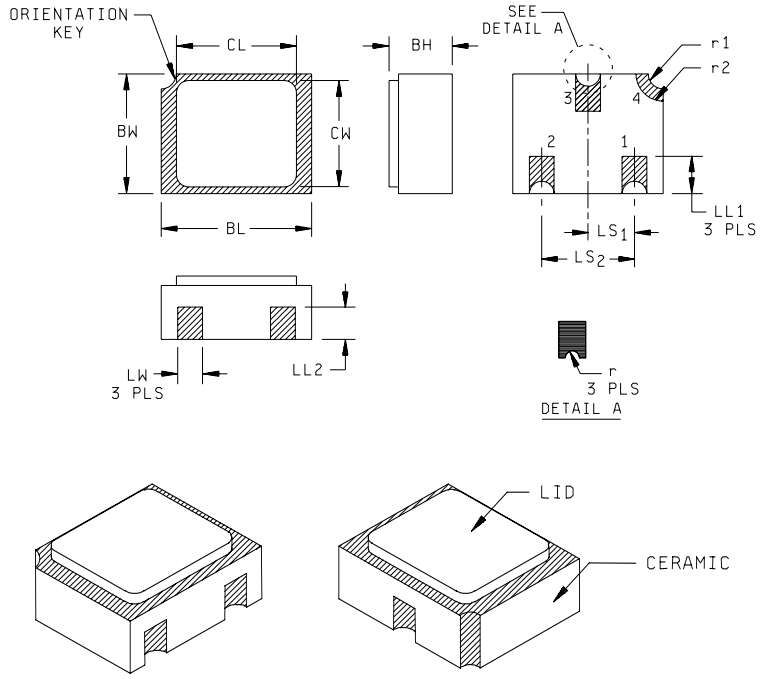
Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7,8
LL	.500	.750	12.70	19.05	7,8
LU	.016	.019	0.41	0.48	7,8
L_1		.050		1.27	7,8
L_2	.250		6.35		7,8
P	.100		2.54		
Q		.040		0.76	5
TL	.028	.048	0.71	1.22	3,4
TW	.036	.046	0.91	1.17	3
r		.010		0.25	10
α	45° TP		45° TP		6
1, 2, 9, 11, 12					





NOTES:
1. Dimension are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TH shall be held for a minimum length of .011 inch (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods or by the gauge and gauging procedure shown in figure 2.
7. Dimension LU applies between L_1 and L_2. Dimension LD applies between L_2 and LL minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
12. Lead 1 = emitter, lead 2 = base, lead 3 = collector.

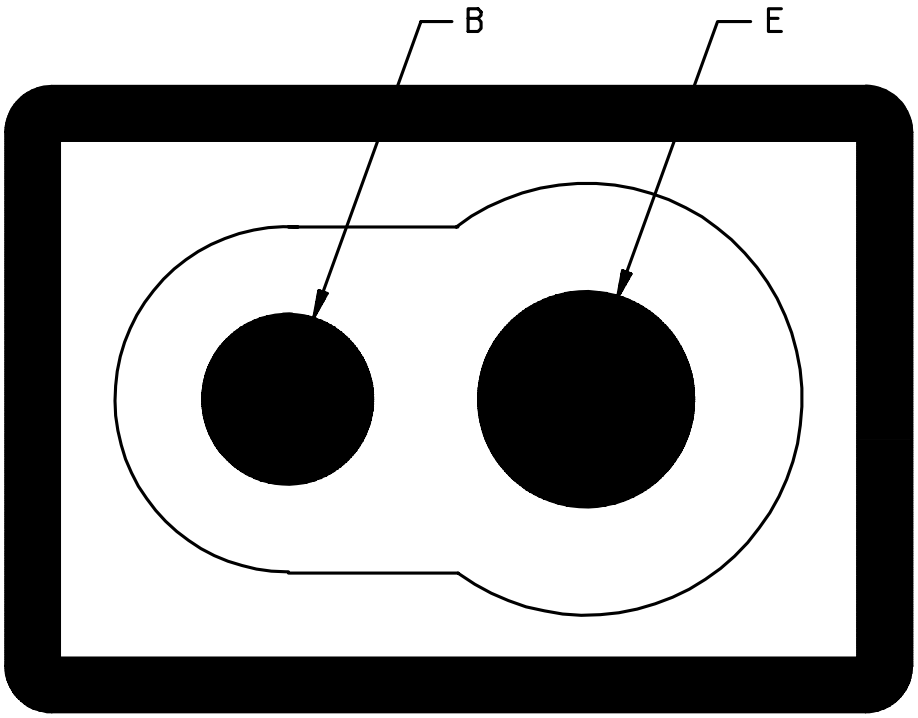
FIGURE 1. Physical dimensions (similar to TO-18).



Symbol	Dimensions				Note	Symbol	Dimensions				Note
	Inches		Millimeters				Inches		Millimeters		
	Min	Max	Min	Max			Min	Max	Min	Max	
BH	.046	.056	1.17	1.42		LS1	.035	.039	0.89	0.99	
BL	.115	.128	2.92	3.25		LS2	.071	.079	1.80	2.01	
BW	.085	.108	2.16	2.74		LW	.016	.024	0.41	0.61	
CL		.128		3.25		r		.008		0.20	
CW		.108		2.74		r1		.012		0.31	
LL1	.022	.038	0.56	0.96		r2		.022		0.56	
LL2	.017	.035	0.43	0.89							

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions, surface mount (UB version).



NOTES:
1. Chip size..... 15 x 19 mils ±1 mil.
2. Chip thickness ..... 10 ±1.5 mil.
3. Top metal ..... Aluminum 15,000Å minimum, 18,000Å nominal.
4. Back metal..... A. Gold 2,500Å minimum, 3,000Å nominal.
   B. Eutectic Mount – No Gold.
5. Backside..... Collector.
6. Bonding pad ..... B = 3 mils, E = 4 mils diameter.
7. Passivation ..... Si_3N_4 (Silicon Nitride) 2 kÅ min, 2.2 kÅ nom.

FIGURE 3. Physical dimensions, JANHCA and JANKCA die.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

I_{BEX} - - - Base cutoff current (dc) with specified circuit between the collector and emitter.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1 (TO-18), figure 2 (UB surface mount), and figure 3 (die) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.6 Electrical test requirements. The electrical test requirements shall be the subgroups specified in 4.4.2 and 4.4.3 herein.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4, and tables I, II, and III).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.2.2.1 Group E thermal response. With extremely small junction devices such as this one, a true thermal impedance cannot be measure, only calculated. While "thermal response" has been substituted for "thermal impedance" herein, the terms, units and procedure as essentially unchanged. Each supplier shall submit a thermal response ($Z_{\theta JX}$) histogram of the entire qualification lot. The histogram data shall be taken prior to the removal of devices that are atypical for thermal response. Thermal response curves (from $Z_{\theta JX}$ test pulse time to $R_{\theta JX}$ minimum steady-state time) of the best device in the qual lot and the worst device in the qual lot (that meets the supplier proposed screening limit), or from the thermal grouping, shall be submitted. The optimal test conditions and proposed initial thermal response screening limit shall be provided in the qualification report. Data indicating how the optimal test conditions were derived for $Z_{\theta JX}$ shall also be submitted. The proposed maximum thermal response $Z_{\theta JX}$ screening limit shall be submitted. The qualifying activity may approve a different $Z_{\theta JX}$ limit for conformance inspection end-point measurements as applicable**.** Equivalent data, procedures, or statistical process control plans may be used for part, or all, of the above requirements. The approved thermal response conditions and limit for $Z_{\theta JX}$ shall be used by the supplier in screening and table I, subgroup 2. The approved thermal resistance conditions for $R_{\theta JX}$ shall be used by the supplier for conformance inspection. For product families with similar thermal characteristics based on the same physical and thermal die, package, and construction combination (thermal grouping), the supplier may use the same thermal response curves.

* 4.3 Screening (JANS, JANTX and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal response, method 3131 of MIL-STD-750, see 4.3.3.	Thermal response, method 3131 of MIL-STD-750, see 4.3.3.
9	h_{FE3}, I_{CBO2}	Not applicable
11	I_{CBO2}; h_{FE3}; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater, Δh_{FE3} = 25 percent change from initial value	I_{CBO2} and h_{FE3}
12	See 4.3.1	See 4.3.1
13	Subgroups 2 and 3 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE3} = 25 percent change from initial value.	Subgroup 2 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE3} = 25 percent change from initial value.

(1) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: T_A = room ambient as defined in 4.5 of MIL-STD-750; V_{CB} = 10 - 30 V dc (10 V dc for JANS); P_T = 360 mW. NOTE: No heat sink or forced air-cooling on the devices shall be permitted.

4.3.2 Screening JANC. Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500, "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

* 4.3.3 Thermal response. For very small junction devices such as this, the term "thermal response" shall be used in lieu of "thermal impedance" although measurements shall be performed the same way as thermal impedance in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW} (V_C and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μs max. See table II, group E, subgroup 4 herein

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIa (JANS) and table E-VIb (JAN, JANTX, and JANTXV) of MIL-PRF-19500. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein. Delta requirements shall be in accordance with the steps of table III herein as specified in the notes for table III.

* 4.4.2.1 Group B inspection, table E-VIa (JANS) of MIL-PRF-19500.

Subgroup	Method	Conditions
B4	1037	V_{CB} = 10 V dc.
B5	1027	NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample. V_{CB} = 10 V dc, $P_D \geq$ 100 percent of maximum rated P_T (see 1.3). Option 1: 96 hours minimum, sample size in accordance with table E-VIa of MIL-PRF-19500, adjust T_A or P_D to achieve T_J = +275°C minimum. Option 2: 216 hours minimum, sample size = 45, c = 0; adjust T_A or P_D to achieve T_J = +225°C minimum.
B6	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3).

4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action.

Step	Method	Condition
1	1026	Steady-state life: 1,000 hours minimum, V_{CB} = 10 V dc, power shall be applied to achieve T_J = +150°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life: T_A = +150°C, V_{CB} = 80 percent rated voltage, 48 hours minimum. n = 45 devices, c = 0.
3	1032	High-temperature life (non-operating), t = 340 hours, T_A = +200°C. n = 22, c = 0.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.

b. Shall be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the test and conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and in 4.4.3.1 (JANS) and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) requirements shall be in accordance with subgroup 2 of table I herein; delta requirements only apply to subgroup C6.

4.4.3.1 Group C inspection (JANS), table E-VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E; (not applicable for UB devices).
C6	1026	1,000 hours at V_{CB} = 10 V dc; power shall be applied to achieve T_J = +150°C minimum and a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3 n = 45, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.

4.4.3.2 Group C inspection (JAN, JANTX, and JANTXV), table E-VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E; not applicable for UB devices.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3).
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests herein for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table II herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein; delta measurements shall be in accordance with the applicable steps of table III.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Collector-base time constant. This parameter may be determined by applying an rf signal voltage of 1.0 volt (rms) across the collector-base terminals, and measuring the ac voltage drop (V_{eb}) with a high impedance rf voltmeter across the emitter-base terminals. With f = 31.8 MHz used for the 1.0 V signal, the following computation applies; $r_b'C_c$ (ps) = 5 x V_{eb} (millivolts), see figure 10.

* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1 2/						
Visual and mechanical examination	2071					
Solderability 3/ 4/	2026	n = 15 leads, c = 0				
Resistance to solvents 3/ 4/ 5/	1022	n = 15 devices, c = 0				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles, n = 22 devices, c = 0				
Hermetic seal 4/ 6/ Fine leak Gross leak	1071	n = 22 devices, c = 0				
Electrical measurements 4/		Table I, subgroup 2				
Bond strength 3/ 4/	2037	Precondition T_A = +250°C at t = 24 hrs or T_A = +300°C at t = 2 hrs n = 11 wires, c = 0				
Decap internal visual (design verification) 4/	2075	n = 4 devices, c = 0				
Subgroup 2						
Thermal response	3131	See 4.3.3	$Z_{\theta JX}$			°C/W
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 60 V dc	I_{CBO1}		10	µA dc
Emitter to base cutoff current	3026	Bias condition D; V_{EB} = 5 V dc	I_{EBO}		10	µA dc
Breakdown voltage collector - emitter	3011	Bias condition D; I_C = 10 mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	60		V dc
Collector - base cutoff current	3036	Bias condition D; V_{CB} = 40 V dc	I_{CBO2}		20	nA dc
Collector - emitter cutoff current	3041	Bias condition A; V_{BE} = 3.0 V dc, V_{CE} = 40 V dc	I_{CEX1}		20	nA dc
Base cutoff current	3041	Bias condition A; V_{BE} = 3.0 V dc; V_{CE} = 40 V dc	I_{BEX}		50	nA dc

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Forward-current transfer ratio	3076	V_{CE} = 1.0 V dc; I_C = 0.1 mA dc	h_{FE1}			
2N3250A, 2N3250AUB				40		
2N3251A, 2N3251AUB				80		
Forward-current transfer ratio	3076	V_{CE} = 1.0 V dc; I_C = 1.0 mA dc	h_{FE2}			
2N3250A, 2N3250AUB				45		
2N3251A, 2N3251AUB				90		
Forward-current transfer ratio	3076	V_{CE} = 1.0 V dc; I_C = 10 mA dc, pulsed (see 4.5.1)	h_{FE3}			
2N3250A, 2N3250AUB				50	150	
2N3251A, 2N3251AUB				100	300	
Forward-current transfer ratio	3076	V_{CE} = 1.0 V dc; I_C = 50 mA dc, pulsed (see 4.5.1)	h_{FE4}			
2N3250A, 2N3250AUB				15		
2N3251A, 2N3251AUB				30		
Current gain linearity		$\frac{\lvert h_{FE3} - h_{FE1} \rvert}{h_{FE3}} \; x \; 100$	h_{FE}			
2N3250A, 2N3250AUB					40	%
2N3251A, 2N3251AUB					30	%
Collector - emitter saturated voltage	3071	I_C = 10 mA dc; I_B = 1.0 mA dc	$V_{CE(SAT)1}$		0.25	V dc
Collector - emitter saturated voltage	3071	I_C = 50 mA dc; I_B = 5.0 mA dc; pulsed (see 4.5.1)	$V_{CE(SAT)2}$		0.50	V dc

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Base - emitter saturated voltage	3066	Test condition A; I_C = 10 mA dc; I_B = 1.0 mA dc	$V_{BE(SAT)1}$	0.60	0.90	V dc
Base - emitter saturated voltage	3066	Test condition A; I_C = 50 mA dc; I_B = 5.0 mA dc; pulsed (see 4.5.1)	$V_{BE(SAT)2}$		1.20	V dc
Subgroup 3						
High-temperature operation:		T_A = +150°C				
Collector - emitter cutoff current	3041	Bias condition A; V_{CE} = 40 V dc; V_{BE} = 3.0 V dc	I_{CEX2}		20	µA dc
Low-temperature operation:		T_A = -55°C				
Forward-current transfer ratio	3076	V_{CE} = 1.0 V dc; I_C = 1.0 mA dc	h_{FE5}			
2N3250A, 2N3250AUB				20		
2N3251A, 2N3251AUB				40		
Subgroup 4						
Small-signal short-circuit forward-current transfer ratio	3206	V_{CE} = 10 V dc; I_C = 1 mA dc; f = 1 kHz	h_{fe}			
2N3250A,				50	200	
2N3250AUB,				50	200	
2N3251A,				100	400	
2N3251AUB				100	400	
Magnitude of common emitter small-signal short-circuit forward-current transfer ratio	3306	V_{CE} = 20 V dc; I_C = 10 mA dc; f = 100 MHz	$\lvert h_{fe} \rvert$			
2N3250A, 2N3250AUB				2.5	9.0	
2N3251A, 2N3251AUB				3.0	9.0	
Open circuit output capacitance	3236	V_{CB} = 10 V dc; I_E = 0 100 kHz ≤ f ≤ 1 MHz	C_{obo}		6	pF

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 4 - Continued						
Input capacitance (output open-circuited)	3240	V_{EB} = 1.0 V dc; I_C = 0; 100 kHz ≤ f ≤ 1 MHz	C_{ibo}		8	pF
Collector-base time constant		V_{CE} = 20 V dc; I_C = 10 mA dc; f = 31.8 MHz; (see 4.5.2 and figure 10)	$r_b'C_c$	5	250	ps
Noise figure	3246	V_{CE} = 5.0 V dc; I_C = 100 μA dc; Rg = 1 kΩ; f = 100 Hz	NF		6	dB
Pulse response:						
On-time	3251	Test condition A; I_C = 10 mA dc; I_{B1} = 1.0 mA dc; (see figure 10)	t_{on}		70	ns
Off time	3251	Test condition A; I_C = 10 mA dc; I_{B1} = I_{B2} = 1.0 mA dc (see figure 12)	t_{off}			
2N3250A, 2N3250AUB					250	ns
2N3251A, 2N3251AUB					300	ns
Small-signal open circuit reverse-voltage transfer ratio	3211	V_{CE} = 10 V dc; I_C = 1.0 mA dc; f = 1 kHz	h_{re}			
2N3250A, 2N3250AUB					10	x 10^{-4}
2N3251A, 2N3251AUB					20	x 10^{-4}
Small-signal short circuit input impedance	3201	V_{CE} = 10 V dc; I_C = 1.0 mA dc; f = 1 kHz	h_{ie}			
2N3250A, 2N3250AUB				1	6	kΩ
2N3251A, 2N3251AUB				2	12	kΩ

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 4 - Continued						
Small-signal open circuit output admittance		V_{CE} = 10 V dc; I_C = 1.0 mA dc; f = 1 kHz	h_{oe}			
2N3250A, 2N3250AUB				4	40	µmhos
2N3251A, 2N3251AUB				10	60	µmhos

1/ For sampling plan see MIL-PRF-19500.
2/ For resubmission of failed test in subgroup 1 of table I, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
3/ Separate samples may be used.
4/ Not required for JANS devices.
5/ Not required for laser marked devices.
6/ This hermetic seal test is an end-point to temp-cycling in addition to electrical measurements.

* TABLE II. Group E inspection (all quality levels) - for qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 2			45 devices c = 0
Intermittent life	1037	V_{CB} = 10 V dc, 6,000 cycles, forced air cooling allowed on cooling cycle only.	
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 4			
Thermal resistance	3131	The following applies for qualification for $R_{\theta JSP(AM)}$ and $R_{JSP(IS)}$ can be calculated but shall be measured once in the same package with a similar die size to confirm calculations (can apply to multiple specification sheets).	15 devices, c = 0
Thermal impedance curves		See 4.2.2.1.	
Subgroup 5			
Not applicable			
Subgroup 6			3 devices
ESD	1020		
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B.	

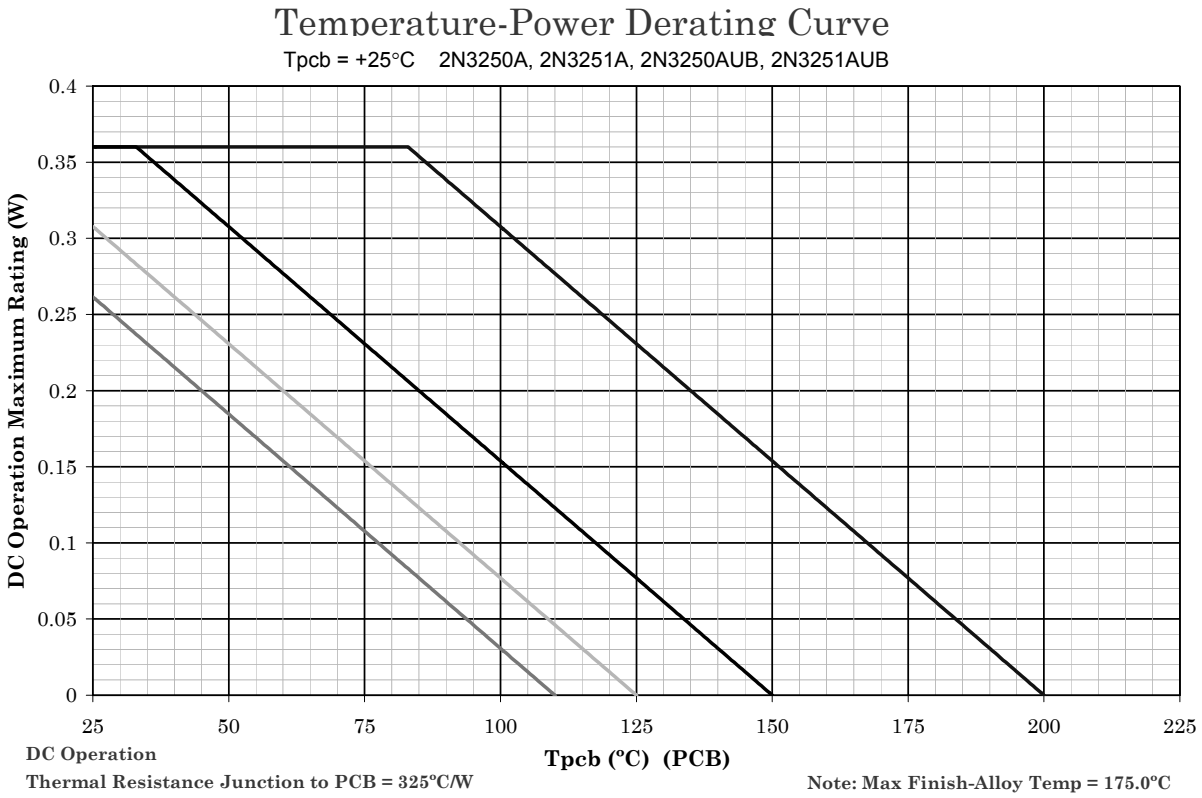
TABLE III. Group B and C delta measurements. 1/ 2/ 3/

Step	Inspection	MIL-STD-750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
1.	Forward-current transfer ratio	3076	V_{CE} = 1.0 V dc; I_C = 10 mA dc; pulsed (see 4.5.1)	Δh_{FE3}	±25 percent change from initial value.		
2.	Collector - base cutoff current	3036	Bias condition D; V_{CB} = 40 V dc	ΔI_{CBO2}	100 percent of initial value or 5 nA dc, whichever is greater.		
3.	Collector - emitter voltage (saturated)	3071	I_C = 50 mA dc; I_B = 5.0 mA dc	$\Delta V_{CE(Sat)2}$	50 mV dc change from initial value.		

1/ The delta measurements for table E-VIa (JANS) of MIL-PRF-19500 are as follows:
a. Subgroup 4, see table III herein, step 3.
b. Subgroup 5, see table III herein, steps 1, 2, and 3.

2/ The delta measurements for table E-VIb (JAN, JANTX, and JANTXV) of MIL-PRF-19500 are as follows: Subgroups 3 and 6, see table III herein, step1.

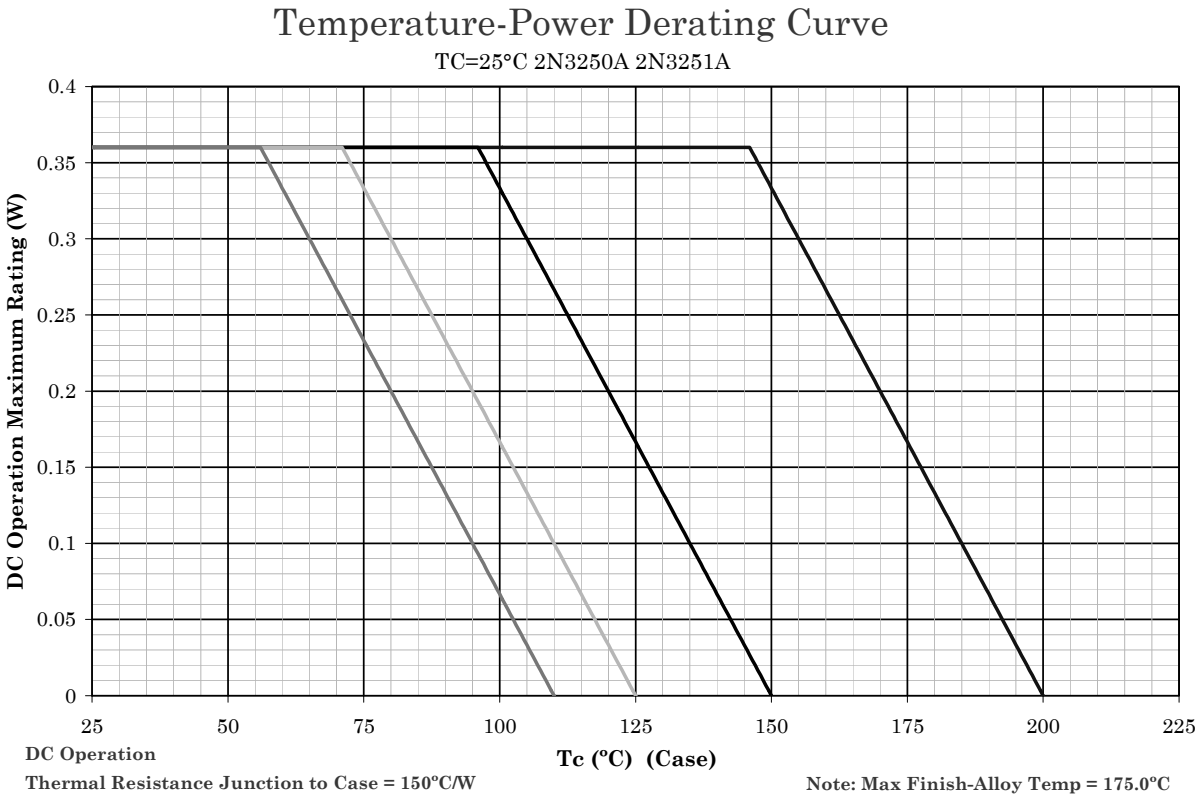
3/ The delta measurements for table E-VII of MIL-PRF-19500 are as follows: Subgroup 6, see table III herein, steps 1 and 2 (for JANS) and 1 (for JAN, JANTX, and JANTXV).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curves chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

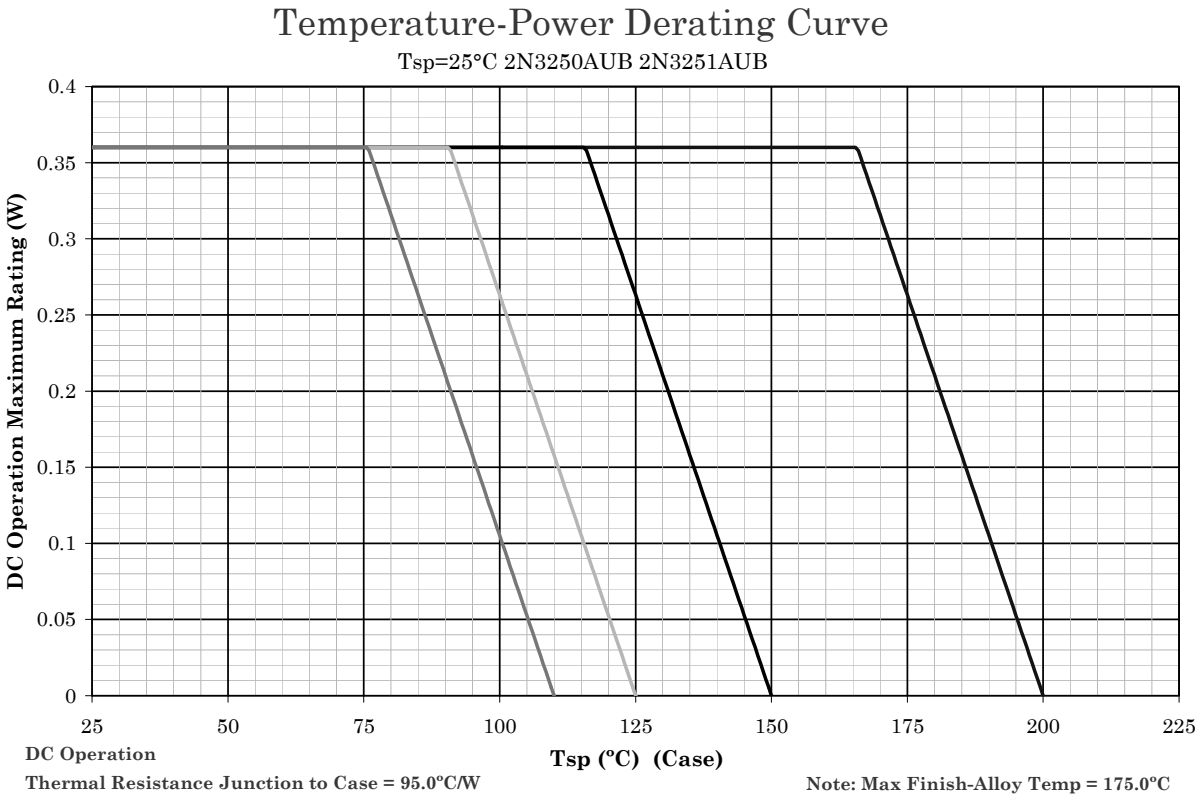
FIGURE 4. Derating for all devices ($R_{\theta JPCB}$) for all parts.



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curves chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

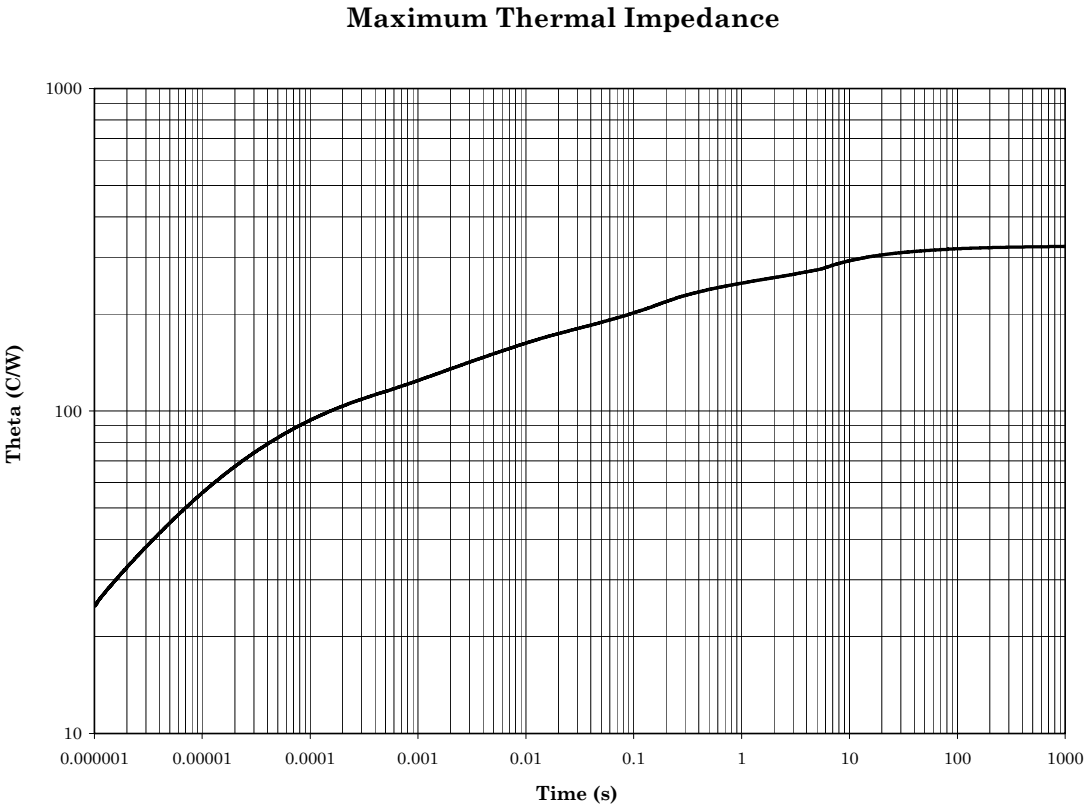
FIGURE 5. Derating for all devices ($R_{\theta JC}$) for all parts.



NOTES:

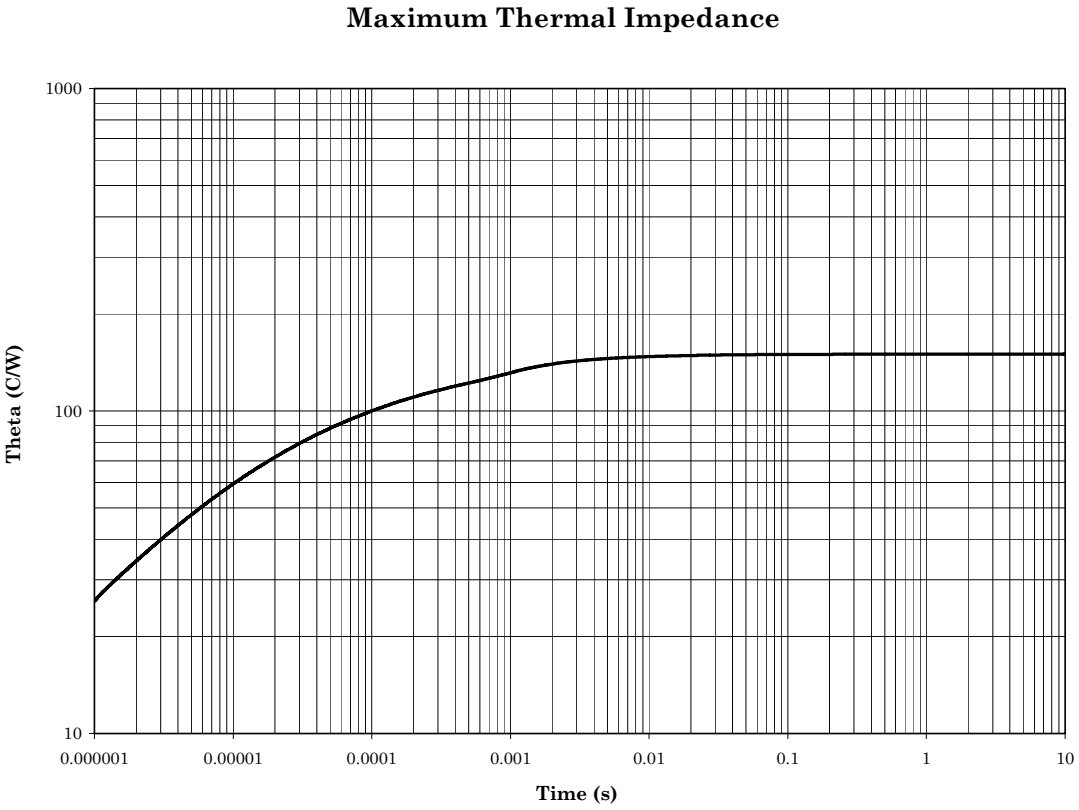
1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curves chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 6. Derating for all devices ($R_{\theta JSP}$) for all parts.



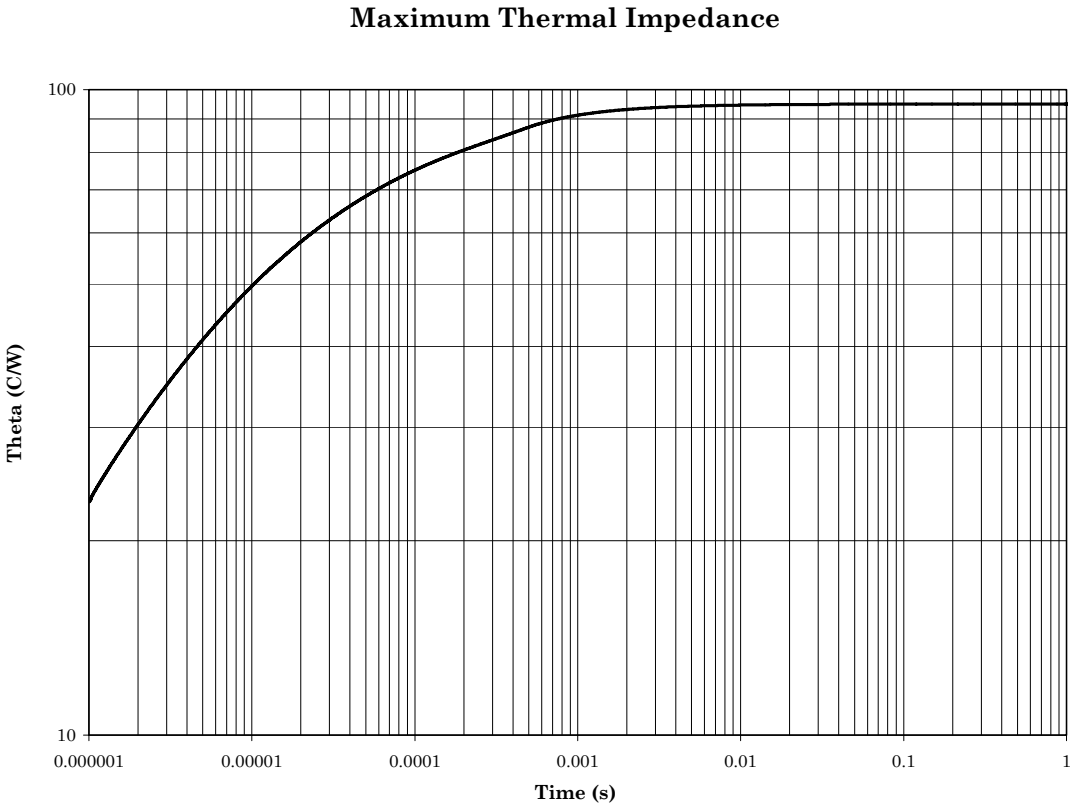
Resistance $R_{\theta JA}$ = 325°C/W.

FIGURE 7. Thermal impedance graph ($R_{\theta JA}$) for 2N3250A and 2N3251A.



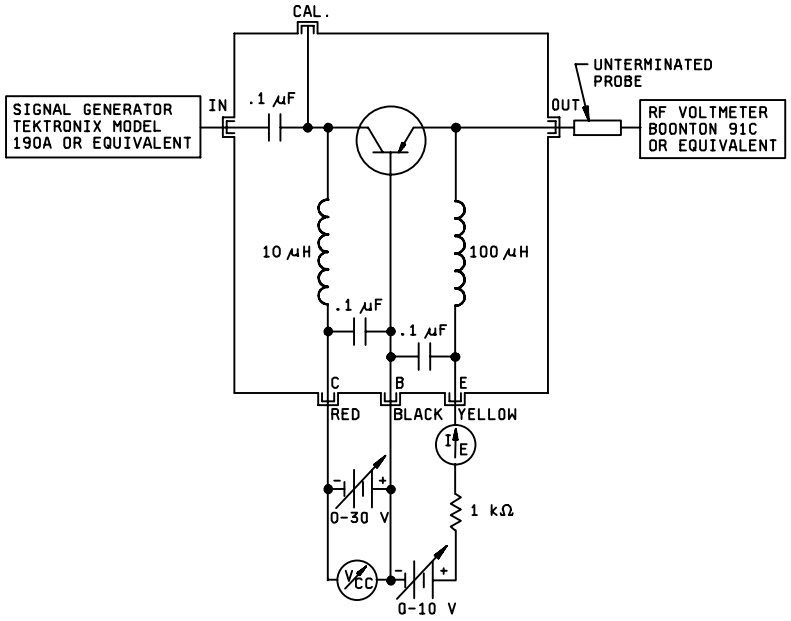
Resistance $R_{\theta JC}$ = 150°C/W.

FIGURE 8. Thermal impedance graph ($R_{\theta JC}$) for 2N3250A and 2N3251A.



Resistance $R_{\theta JSP}$ = 95°C/W.

FIGURE 9. Thermal impedance graph ($R_{\theta JSP}$) for 2N3250AUB and 2N3251AUB.

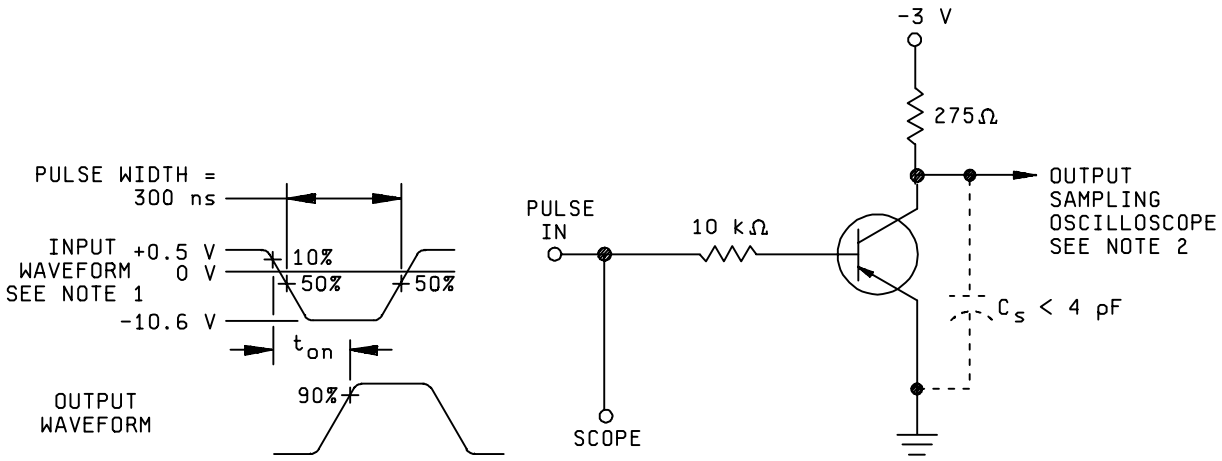


Procedure:

1. Set signal generator to 31.8 MHz and connect to "IN" connector on test jig.
2. Connect low voltage dc power supplies as shown. A 1 K ohm resistor should be placed in series with the emitter power supply to prevent damage to transistors being tested.
3. Set collector supply for V_{CE} = -20 V dc, and emitter supply for I_C = -10 mA.
4. Connect RF voltmeter with unterminated probe adapter to "CAL" connector on test jig. Adjust signal generator until RF voltage is 1 volt. (NOTE: Decade switching of voltmeter should be accurate from 1 mV to 3 volts. If not, input voltage may be set using voltage dividers, utilizing lower scales of the RF voltmeter. If this is done, the voltage dividers should be left in place when the voltmeter is removed, as they constitute a load on the input of the circuit.)
5. Remove RF voltmeter from "CAL" connector and connect to "OUT" connector. Meter will now read $r_b'C_c$ as follows:

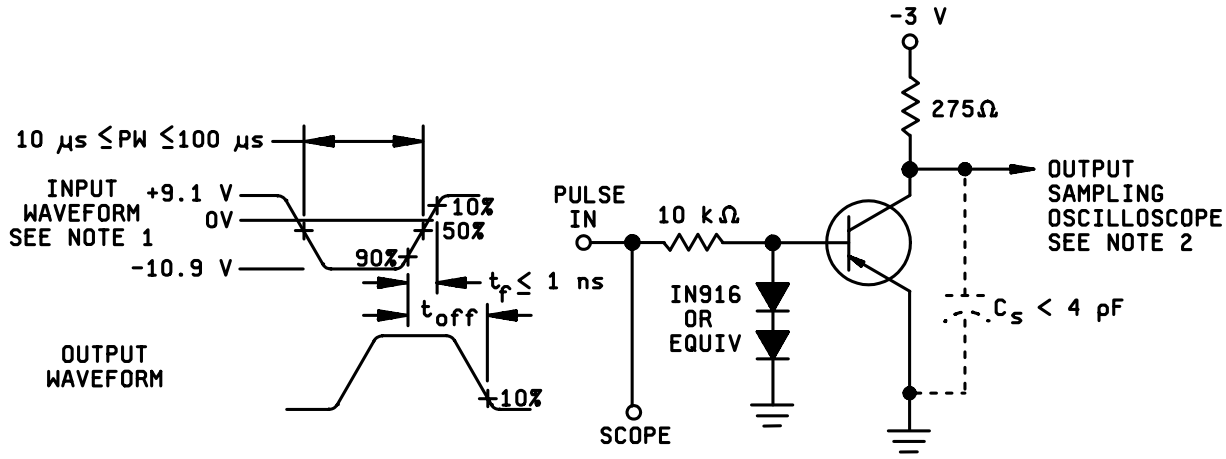
Meter range full scale
3 mV
10 mV
30 mV
.1 volt

FIGURE 10. Collector-base time constant test circuit (an equivalent circuit may be used).



NOTES:
1. The rise time (t_r) of the applied pulse shall be ≤ 1.0 ns, duty cycle ≤ 2 percent, and the generator source Z shall be 50Ω.
2. Sampling oscilloscope: Z_{IN} ≥ 100 kΩ; rise time(t_r) ≤ .1 ns.

FIGURE 11. Delay and rise time, test circuit.



NOTES:
1. The rise time (t_r) of the applied pulse shall be ≤ 1.0 ns, duty cycle ≤ 2 percent, and the generator source Z shall be 50Ω.
2. Sampling oscilloscope: Z_{IN} ≥ 100 kΩ; rise time (t_r) ≤ .1 ns.

FIGURE 12. Storage and fall time, test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil.

6.4 Suppliers of JANHC and JANKC die. The qualified JANHC/JANKC suppliers with the applicable letter version (example, JANHCA2N3250A) will be identified on the QML.

JANC ordering information	
PIN	Manufacturer
	43611
2N3250A, AUB 2N3251A, AUB	JANHCA2N3250A JANHCA2N3251A
2N3250A, AUB 2N3251A, AUB	JANKCA2N3250A JANKCA2N3251A

6.5 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

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